TDA19971

Single HDMI 1.4b receiver with digital processing

Rev. 3 — 22 March 2013 Product data sheet

1. General description

The TDA19971 HDMI receiver proposes one HDMI input and standard video bus output optimized for STB and PVR system integration. The TDA19971 offers High Definition (HD) video resolutions up to 1080p50/60 or WUXGA and HD audio formats up to 8 channels such as DTS HD and Dolby True HD while keeping advanced sleep modes power management.

This chip optionally includes HDCP 1.4 engine with pre-programmed keys stored into an internal non-volatile memory to provide highly secured solution and simplify manufacturing process.

This chip features several HDMI 1.4b options such as 3D format up to 1080p50/60, Deep Colors up to 36 bits per pixel and extended colorimetry. The TDA19971 integrates 8 kV system ESD protections and non-volatile memory for EDID storage to minimize BOM.

An optimized auto-adaptative equalizer increases TDA19971 robustness for poor quality signals. The TDA19971 is delivered with software drivers for Linux, Windows and RTOS easy to implement and to configure.

To build a complete system with the TDA19971, refer to the corresponding application notes. Evaluation platforms and user guide are available on request to NXP support.

2. Features and benefits

- HDMI 1.4b receiver (1 input), DVI 1.0, CEA-861-D and HDCP 1.4 standards, up to the HDMI frequency of 235 MHz
  - Auto-adaptative equalizer
  - Deep Color (30 bits per pixel and 36 bits per pixel)
  - HPD 4 V level for HEAC feature, HPD automatic management
  - CEC feature
  - Embedded EDID non-volatile memory: EDID readable with +5 V from the source
  - DDC-bus inputs: 5 V tolerant and bit rate up to 400 kbit/s, support threshold V_{IL} = 1.5 V (30 % of 5 V) and V_{IH} = 2.3 V (70 % of 3.3 V)
  - All HDTV formats up to 1920 × 1080p at 50/60 Hz with support for reduced blanking
  - 3D formats including all primary formats up to 1920 × 1080p at 30 Hz Frame Packing and 1920 × 1080p at 60 Hz Side-by-Side and Top-and-Bottom
  - PC formats up to UXGA (1600 × 1200p at 60 Hz) and WUXGA (1920 × 1200p at 60 Hz)
- Optional HDCP:

- Repeater capability (requires software driver)
- Embedded non-volatile memory storage of HDCP keys

- Video
  - Integrated downsampling-by-two with selectable filters on Cb and Cr channels for 4:2:2 mode
  - Programmable color space conversion: RGB or YCbCr input signal into YCbCr or RGB output
  - Color gamut metadata packet with interrupt on each update, readable via the I^2C-bus
  - Internal 36-bit video processing
  - Video output single or dual rate for video interface
  - Frame and field detection for interlaced video signal
  - Sync timing measurements for automatic format recognition
  - Improved system for measurements of blanking and video active area allowing an accurate recognition of PC and TV formats
  - Output formats: RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar based on the ITU-R BT.601 standard and YCbCr 4:2:2 ITU-R BT.656
  - 8 bits, 10 bits or 12 bits per component output formats selectable using the I^2C-bus and output mapping fully programmable
  - Internal video and audio patterns generator
- Audio
  - Audio clock generation from Xtal: 128 f_s, 256 f_s, 512 f_s and Fs = 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 172.4 kHz, 192 kHz
  - Up to four S/PDIF or I^2S-bus outputs (8 channels) at a sampling rate up to 192 kHz with IEC 60958/IEC 61937 stream
  - HBR streams (compatible with DTS-HD master audio and Dolby TrueHD up to 8 channels due to HBR packet for stream with a frame rate up to 768 kHz) support
  - Improved audio clock generation using an external reference clock
  - Embedded audio pop noise remover
  - S/PDIF or I^2S-bus up to 8 channels
- General
  - Embedded ESD protection according to IEC 61000-4-2 class 4 (±8 kV contact, ±15 kV air)
  - Controllable using the I^2C-bus; 5 V tolerant and bit rate up to 400 kbit/s
  - I^2C-bus adjustable timing of video port
  - LV-TTL outputs
  - Low-power mode
  - CMOS process
  - 1.8 V and 3.3 V power supplies
  - 0 °C, 70 °C temperature range
  - Packages: HVQFN72 10 mm × 10 mm pitch 0.5 mm
    (other package option could be considered on request)
  - Low-power: clock gating on each video block, optional 2.5 V supply on audio/video output instead of 3.3 V for SoC

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3. Applications

- Projector
- STB
- Tablet
- Monitor
- AVR/VCR/AVN
- Video conference
- Media box
- ADSL boxes
- HDMI/HDCP repeater

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HDMI input pins: RX_C+, RX_C–						
f_{clk}	clock frequency		20	-	235	MHz
Clock output timing pins: V_CLK and A_CLK						
$f_{clk(max)}$	maximum clock frequency	pin V_CLK	-	-	165	MHz
		pin A_CLK	-	-	24.5	MHz
Supplies						
$V_{DDAH(RX)(3V3)}$	receiver HDMI analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDA(PLL)(3V3)}$	PLL analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDAH(RX)(1V8)}$	receiver HDMI analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDA(DCPLL)(1V8)}$	deep color PLL analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)	standard 3.3 V I/O	3	3.3	3.6	V
		standard 2.5 V I/O	2.25	2.5	2.75	V
$V_{DDA(AUDPLL)(1V8)}$	audio PLL analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDA(XTAL)(1V8)}$	crystal analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.65	1.8	1.95	V
P_{cons}	power consumption	Operating mode [1]				
		720p at 60 Hz	-	500	-	mW
		1080p at 60 Hz	-	636	-	mW
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	799	-	mW
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	-	mW
		pin RSTN = LOW	-	19	-	mW
		Idle mode; I^2C-bus; EDID; activity detection and HDCP [2] memory power-up	-	45	-	mW

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[1] At 30 % activity on video port output, add 132 mW for an HDMI input with typical TMDS swing.

[2] HDCP decoding is only supported by the TDA19971A.

5. Ordering information

Table 2. Package information

Type number	Package		
	Name	Description	Version
TDA19971AHN/C1	HVQFN72	plastic thermal enhanced very thin quad flat package; no leads; 72 terminals; body 10 × 10 × 0.85 mm	SOT813-4
TDA19971BHN/C1			

Table 3. Ordering information

Type number	HDCP	Package type	ROM code
TDA19971AHN/C1	yes	HVQFN72	TDA19971AHN/C1XX[1]
TDA19971BHN/C1	no	HVQFN72	-

[1] XX depends on the customer, to get specific value of XX contact NXP sales.

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6. Block diagram

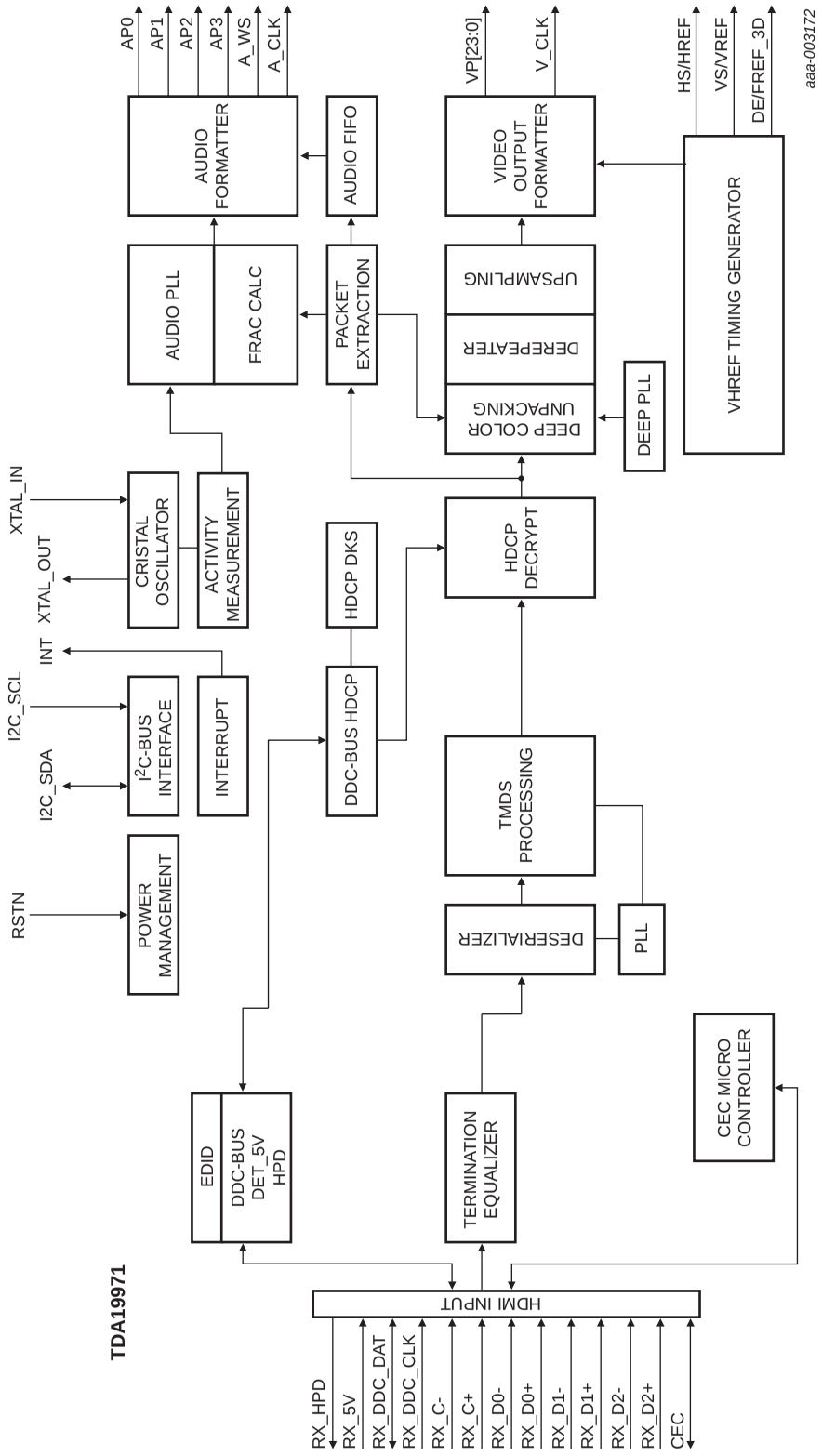

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

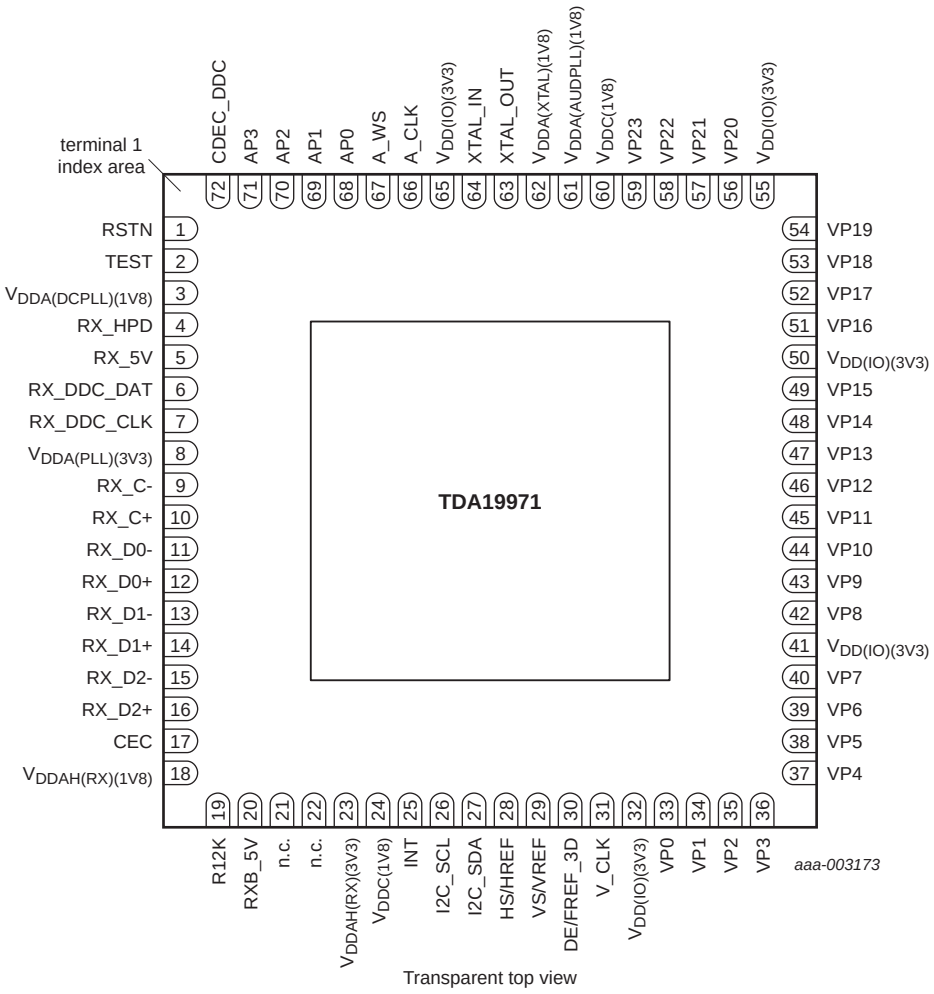

Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
RSTN	1	I	reset (active LOW)
TEST	2	I	reserved for test; connect to digital inputs ground
$V_{DDA(DCPPLL)(1V8)}$	3	P	Deep Color PLL analog supply voltage; 1.8 V
RX_HPD	4	O	hot plug detect; 5 V tolerant
RX_5V	5	I	input HDMI +5 V
RX_DDC_DAT	6	I/O	HDMI input/output DDC-bus serial data; open-drain; 5 V tolerant

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Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
RX_DDC_CLK	7	I	HDMI input DDC-bus serial clock; open-drain; 5 V tolerant
$V_{DDA(PLL)(3V3)}$	8	P	PLL analog supply voltage; 3.3 V
RX_C–	9	I	HDMI input negative clock channel
RX_C+	10	I	HDMI input positive clock channel
RX_D0–	11	I	HDMI input negative data channel 0
RX_D0+	12	I	HDMI input positive data channel 0
RX_D1–	13	I	HDMI input negative data channel 1
RX_D1+	14	I	HDMI input positive data channel 1
RX_D2–	15	I	HDMI input negative data channel 2
RX_D2+	16	I	HDMI input positive data channel 2
CEC	17	I/O	CEC connection (open-drain) to HDMI connector
$V_{DDAH(RX)(1V8)}$	18	P	receiver HDMI analog supply voltage; 1.8 V
R12K	19	I	termination resistor control
RXB_5V	20	-	pin test for debug; not connected
n.c.	21	-	not connected
n.c.	22	-	not connected
$V_{DDAH(RX)(3V3)}$	23	P	receiver HDMI analog supply voltage; 3.3 V
$V_{DDC(1V8)}$	24	P	core supply voltage; 1.8 V
INT	25	O	interrupt request
I2C_SCL	26	I/O	I^2C-bus serial clock input/output
I2C_SDA	27	I/O	I^2C-bus serial data input/output
HS/HREF	28	O	output horizontal synchronization or reference output
VS/VREF	29	O	output vertical synchronization or reference output
DE/FREF_3D	30	O	data enable output or field reference output
V_CLK	31	O	video clock output
$V_{DD(IO)(3V3)}$	32	P	input/output supply voltage; 3.3 V
VP0	33	O	video port output bit 0
VP1	33	O	video port output bit 1
VP2	35	O	video port output bit 2
VP3	36	O	video port output bit 3
VP4	37	O	video port output bit 4
VP5	38	O	video port output bit 5
VP6	39	O	video port output bit 6
VP7	40	O	video port output bit 7
$V_{DD(IO)(3V3)}$	41	P	input/output supply voltage; 3.3 V
VP8	42	O	video port output bit 8
VP9	43	O	video port output bit 9
VP10	44	O	video port output bit 10
VP11	45	O	video port output bit 11
VP12	46	O	video port output bit 12
VP13	47	O	video port output bit 13

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Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
VP14	48	O	video port output bit 14
VP15	49	O	video port output bit 15
$V_{DD(IO)(3V3)}$	50	P	input/output supply voltage; 3.3 V
VP16	51	O	video port output bit 16
VP17	52	O	video port output bit 17
VP18	53	O	video port output bit 18
VP19	54	O	video port output bit 19
$V_{DD(IO)(3V3)}$	55	P	input/output supply voltage; 3.3 V
VP20	56	O	video port output bit 20
VP21	57	O	video port output bit 21
VP22	58	O	video port output bit 22
VP23	59	O	video port output bit 23
$V_{DDC(1V8)}$	60	P	core supply voltage; 1.8 V
$V_{DDA(AUDPLL)(1V8)}$	61	P	audio PLL analog supply voltage; 1.8 V
$V_{DDA(XTAL)(1V8)}$	62	P	crystal analog supply voltage; 1.8 V
XTAL_OUT	63	O	crystal oscillator output
XTAL_IN	64	I	crystal oscillator input
$V_{DD(IO)(3V3)}$	65	P	input/output supply voltage; 3.3 V
A_CLK	66	O	audio clock output
A_WS	67	O	audio word select output
AP0	68	O	audio port 0 output
AP1	69	O	audio port 1 output
AP2	70	O	audio port 2 output
AP3	71	O	audio port 3 output
CDEC_DDC	72	O	internal supply voltage regulator decoupling capacitor; 1.8 V
Exposed die pad	-	G	exposed die pad; connect to ground

[1] P = power supply; G = ground; I = input; O = output and I/O = input/output.

8. Functional description

The source sends digital data stream to the TDA19971 HDMI input. The TDA19971 converts HDMI signal into parallel digital data for use by media and video signal processing integrated circuits. Data streams can be decoded with or without HDCP protection.

Outputs from the TDA19971 can be RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar format based on the ITU-R BT.601 standard or YCbCr 4:2:2 based on the ITU-R BT.656 format. Input can be both progressive or interlaced formats. The TDA19971 integrates a color space conversion block, downsampling filters and embedded timing codes function. In addition, the HDCP (TDA19971A only) repeater function enables other HDMI devices to be connected to form an extended “total application”.

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8.1 Software drivers

Software drivers are provided for easy configuration and use of the TDA19971. These drivers can be integrated with a large range of processors, with or without operating system. They control activity detection, video mode identification, color conversion, low-power modes, HDCP (TDA19971A only) and Info Frame notification.

8.2 HDMI

8.2.1 HDMI input

HDMI input can be self-controlled using embedded activity detection system or controlled by the I^2C-bus. The HDMI receiver input is defined by pins RX_D0+, RX_D0−, RX_D1+, RX_D1−, RX_D2+, RX_D2−, RX_C+, RX_C−, RX_DDC_DAT, RX_DDC_CLK, RX_5V and RX_HPD.

8.2.2 Termination resistance control

The HDMI receiver input contains a termination resistance control set by an external resistor connected between pins R12K and $V_{DDAH(RX)(3V3)}$. Typically, the characteristic impedance is 50 Ω and the default value of the external terminal control resistor is 12 kΩ ± 1 %.

The termination resistors can be disconnected from the 3.3 V supply to remove the common mode voltage via I^2C-bus access and/or when RX_HPD is LOW.

8.2.3 Equalizer

The auto-adaptative equalizer automatically measures and selects the settings which provide the best signal quality for each frequency and each cable characteristics. Signals from short cables with very low TMDS clock frequencies (20 MHz) to long cables (up to 20 m) at high TMDS clock frequencies (235 MHz) are easily managed by the equalizer. The equalizer is fully automatic and so does not need any external control.

8.2.4 Embedded EDID memory management

The size of the EDID memory is 256 bytes.

EDID content programming could be performed using the non-volatile memory when the content is fixed or directly by the I^2C-bus when the content depends of system configuration (for example, EDID content of the attached sink device). The EDID memory can be powered by +5 V from the source. In low-power mode, the EDID memory remains active. Access from pins RX_DDC_DAT and RX_DDC_CLK is independent of other supplies. So, the source has access to the EDID memory when TDA19971 is not powered by the 3.3 V and 1.8 V.

Remark: the maximum number of write cycles for the non-volatile memory is 200 cycles. And the write process shall be executed only in Idle mode (no HDMI input). But there is no limitation when the EDID content is programmed directly by the I^2C-bus.

8.2.5 Activity detection

An internal, fully programmable, frequency filter controls activity detection. It monitors only the activity on the HDMI input with a frequency range between f_{min} (22.5 MHz) and f_{max} (235 MHz).

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This activity detection can generate an interrupt enabling users to manage HDMI input.

The TMDS frequency can be read by I²C-bus, however, the precision of the value depends on crystal oscillator accuracy.

8.2.6 Display Data Channel (DDC)

Pins RX_DDC_DAT and RX_DDC_CLK are compatible with the I²C-bus specification in Fast-mode (400 kHz).

In addition, pins RX_DDC_DAT and RX_DDC_CLK are high-impedance when the device is not 5 V supplied. Pins RX_DDC_DAT and RX_DDC_CLK support from 3.3 V to 5 V external pull-up. V_{IL} = 1.5 V (30 % of 5 V) and V_{IH} = 2.3 V (70 % of 3.3 V).

Embedded EDID and HDCP modules do not generate clock stretching on DDC.

8.2.7 High-bandwidth digital content protection (TDA19971A only)

The HDMI receiver also contains the HDCP decryption function. The keys provided by the embedded non-volatile memory in encrypted format are decrypted and then stored in the HDCP module. This is particularly suitable for repeater applications. The TDA19971A manages all HDCP repeater functions based on the HDCP 1.4 specification.

No additional CPU processing is required because the authentication phase and the rekey calculation are fully managed by the TDA19971A.

However, in HDCP repeater mode:

- The maximum number of attached devices is 48. It means that the KSV list maximum is 48
- CPU is required to run software drivers

8.3 Video

8.3.1 Color depth unpacking

In Deep Color mode, the TDA19971 receives several fragments of a pixel group at the HDMI link frequency. This block translates the received pixel group into pixels at the pixel frequency. This operation is fully automatic and does not need any external control.

8.3.2 Derepeater

The HDMI source uses pixel repetition to increase the transmitted pixel clock for transmitting video formats at native pixel rates below 25 Mpixel/s or to increase the number of audio sample packets in each line. The derepeater function discards repeated pixels and divides the clock to reproduce the native video format.

8.3.3 Upsample

The HDMI source can use YCbCr 4:2:2 pixel encoding which enables the number of bits allocated per component to be increased up to 12. The upsample function transforms this 12-bit YCbCr 4:2:2 data stream into a 12-bit YCbCr 4:4:4 data stream by repeating or linearly interpolating the chrominance pixels Cb and Cr.

Upsampling mode is selected using the I²C-bus.

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8.3.4 Sync timing measurement

To assist input format recognition, the vertical/horizontal periods and the horizontal pulse width are measured.

8.3.5 Format measurement timing

The TDA19971 includes an improved system for accurate recognition of PC and TV formats. This system measures the parameters of blanking and video active area.

This function can be useful for example when the TDA19971 receives PC format data in HDMI or DVI modes.

8.3.6 Color space conversion

The color space conversion enables an RGB signal from the HDMI input to be converted into a YCbCr signal or converting the YCbCr signal from the HDMI input into an RGB signal. The color space conversion formula is:

$$\begin{bmatrix} YG \\ VR \\ UB \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} CY \\ RV \\ BU \end{bmatrix} + \begin{bmatrix} O11 \\ O12 \\ O13 \end{bmatrix} \right) + \begin{bmatrix} OO1 \\ OO2 \\ OO3 \end{bmatrix} \quad (1)$$

Activation of the color space conversion function, programming of all coefficients and offsets is done using the I^2C-bus.

8.3.7 4:2:2 downsampling filters

These filters downsample the Cb and Cr signals by a factor of 2. A delay has been added to the G/Y channel corresponding to the downsample filters pipeline delay to make sure that the Y channel is in phase with the Cb and Cr channels.

Four different filters, from simple cut to ITU-R BT.601 compliant digital, can be selected using the I^2C-bus.

8.3.8 Range control

The range control function truncates the range of data to remove super-white and super-black pixels at specified ceiling and floor programmable values.

8.3.9 Color depth reduction

The error dispersal rounding (dithering) function can convert the color depth from 30-bit or 36-bit to reduced 30-bit or 24-bit color depth. When dithering is triggered, the TDA19971 applies round, truncate or noise-shaping algorithms.

When the error dispersal rounding function is not used, the data coming from the filter is directly sent to the 4:2:2 formatter. The error dispersal rounding function works only with the active video signal.

8.3.10 4:2:2 formatter

The 4:2:2 formatter contains the YCbCr 4:2:2 semi-planar and the YCbCr 4:2:2 ITU-R BT.656 formatting functions. The selection of these functions is made using the I^2C-bus.

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- In YCbCr 4:2:2 mode: the data frequency for the Y signal is equal to the pixel clock frequency. While the data frequency for the Cb and Cr signals is equal to half the pixel clock frequency
- In semi-planar mode: the output clock should be the same as the pixel clock
- In ITU-R BT.656 mode: the data frequency should be the same as the formatter clock frequency (for example, pixel clock $\times$ 2)

The Start Active Video (SAV) and the End Active Video (EAV) timing reference codes can be included in the data stream based on the HREF, VREF and FREF positions from the VHREF timing generator.

8.3.11 Gamut-related metadata

Gamut-related metadata is an enhanced colorimetry beyond the default standard with higher definition colorimetries. Profile P0 is supported, which means that only one packet per video field is sent. Color gamut boundary data are defined by the standards:

- xvYCC601 (IEC 61966-2-4 – SD) (using YCbCr)
- xvYCC709 (IEC 61966-2-4 – HD) (using YCbCr)
- AdobeYCC601 (IEC 61966-2-5) (using YCbCr)
- AdobeRGB (IEC 61966-2-5) (using RGB)

8.3.12 Video port selection

Each channel can be allocated to a specified video port using the I^2C-bus to optimize board layout at the interface with video processing ICs. For example:

- R, G or B in RGB 4:4:4 8-bit mode on VP[23:0]
- Y, Cb or Cr in YUV 4:4:4 8-bit mode on VP[23:0]
- Y or Cb-Cr in 4:2:2 semi-planar 8-bit mode on VP[15:0]
- Y or Cb-Cr in 4:2:2 semi-planar 10-bit mode Cb-Cr on VP[23:14] and Y on VP[11:2]
- Y or Cb-Cr in 4:2:2 semi-planar 12-bit mode on VP[23:0]
- Cb-Y-Cr-Y in 4:2:2 ITU-R BT.656 8-bit mode on VP[7:0]
- Cb-Y-Cr-Y in 4:2:2 ITU-R BT.656 10-bit mode on VP[9:0]
- Cb-Y-Cr-Y in 4:2:2 ITU-R BT.656 12-bit mode on VP[11:0]

Each video port can be set to high-impedance using the I^2C-bus (default mode).

TDA19971 embeds an output video mapping processor. The aim of this processor is to map the internal signal to any pin mapping and be compatible with any SoC or device receiving the video buses.

The device can also swap and invert bits according to the output mode needed (big endian or little endian digital stream).

8.3.13 Output buffers

The levels of the output buffers are LV-TTL compatible (refer to Table 11 “Characteristics”). Switching the outputs between active and high-impedance is set using the I^2C-bus.

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The output pins HS/REF, VS/VREF and DE/FREF_3D can be set to high-impedance (Z) or forced LOW (L), independently of the timing reference codes.

8.3.14 VHREF timing generator

The VHREF timing generator outputs all of the timing signals used by the device:

- VREF, HREF and FREF signals for SAV, EAV and active video area definition
- VS and HS to change width and position compared with the HDMI input

8.4 Audio

8.4.1 Packet extraction

Information sent during the Data Island periods is extracted from the HDMI data stream. Audio clock regeneration, general control and Info Frames can be read using the I^2C-bus while audio samples are sent to the audio FIFO.

In audio applications, the TDA19971 manages HBR packets for High Bit Rate compressed audio streams (IEC 61937).

The TDA19971 includes a channel status decoder supporting multi-channel reception for audio sample packets. This enables the user to obtain channel status information from the IEC 60958/IEC 61937 stream such as:

- The audio stream type (non-linear as IEC 61937 or L-PCM as IEC 60958)
- Copyright protection
- Sampling frequency

Refer to *IEC 60958/IEC 61937 specifications* for more details.

An update of each Info Frame or the channel status content is indicated by a register bit and the HIGH-to-LOW transition on output interrupt pin INT. This makes CPU polling unnecessary.

Audio pop noise remover is embedded in the audio block. Audio clock output is disabled as soon as TMDS activity is stopped.

8.4.2 Audio PLL

The programming of the audio can be either automatic, using the audio clock regeneration parameters found in the Data Islands or set manually using the I^2C-bus.

All standard audio sampling frequencies 32 kHz, 44.1 kHz, 88.2 kHz, 176.4 kHz, 48 kHz, 96 kHz and 192 kHz are accepted by the device.

8.4.3 Audio formatter

Audio samples can be output in either S/PDIF, I^2S-bus formats. In I^2S-bus mode, the TDA19971 is master with 16 bits or 32 bits per word. In I^2S-bus or S/PDIF modes, up to 8 audio channels can be controlled using the audio port pins (AP0 to AP3 and A_WS). The audio port mapping depends on the channel allocation (see Table 5, Table 6 and Table 7 for detailed information).

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Table 5. Audio port configuration (layout 0)

All audio ports are LV-TTL compatible.

Audio port	Layout 0	
	I²S-bus	**S/PDIF**
AP3		
AP2		
AP1		
AP0	SD	S/PDIF
A_WS	WS (Word Select)	WS[1]
A_CLK	SCK (I²S-bus clock) 64 × f_s[2] 32 × f_s[3]	master clock for S/PDIF[1] 64 × f_s

[1] Can be activated with the I²C-bus (optional).

[2] In 32 bits per word.

[3] In 16 bits per word.

Table 6. Audio port configuration (layout 1)

All audio ports are LV-TTL compatible.

Audio port	Layout 1	
	I²S-bus	**S/PDIF**
AP3	SD3	S/PDIF3
AP2	SD2	S/PDIF2
AP1	SD1	S/PDIF1
AP0	SD0	S/PDIF0
A_WS	WS (Word Select)	WS[1]
A_CLK	SCK (I²S-bus clock) 64 × f_s[2] 32 × f_s[3]	master clock for S/PDIF[1] 64 × f_s

[1] Can be activated with the I²C-bus (optional).

[2] In 32 bits per word.

[3] In 16 bits per word.

Table 7. Audio port configuration for HBR packets

All audio ports are LV-TTL compatible.

Audio port	HBR demultiplexed	
	I²S-bus	**S/PDIF**
AP3	SD[x + 3]	S/PDIF[x + 3]
AP2	SD[x + 2]	S/PDIF[x + 2]
AP1	SD[x + 1]	S/PDIF[x + 1]
AP0	SD[x]	S/PDIF[x]
A_WS	WS (Word Select)	WS[1]
A_CLK	SCK (I²S-bus clock) 64 × f_s (ACR)[2] 32 × f_s (ACR)[3]	master clock for S/PDIF[1] 64 × f_s (ACR)

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[1] Can be activated with the I²C-bus (optional).

[2] In 32 bits per word.

[3] In 16 bits per word.

8.5 General

8.5.1 I²C-bus serial interface

The TDA19971 allows software programming of its internal registers (HDMI or CEC) using the I²C-bus.

To access registers, the TDA19971 uses the I²C-bus. The TDA19971 acts as an I²C-bus slave device. Both Fast-mode (400 kHz) and Standard-mode (100 kHz) are supported by the TDA19971. The slave I²C-bus address is shown in Table 8.

The TDA19971 generates clock stretching on I²C-bus. Main I²C-bus is a slave I²C-bus without clock stretching generation. But I²C-bus from asynchronous page generates clock stretching when CEC module is enabled.

The I²C-bus slave address for the HDMI internal registers is 1001 A2 A1 A0 R/W. Address bit values are stored in the non-volatile configuration memory and enable selection of the slave address. The default slave address value is 1001 000x.

The I²C-bus slave address for asynchronous module, including CEC block, is 0110 1 AS_A1 AS_A0 R/W. Address bit values are stored in the non-volatile configuration memory and enable selection of the slave address. The default slave address value is 0110 100x.

Table 8. Default slave address

Device function	Bit							
	A6	A5	A4	A3	A2	A1	A0	R/W
TDA19971_HDMI	1	0	0	1	A2	A1	A0	1/0
TDA19971_AS	0	1	1	0	1	AS_A1	AS_A0	1/0

I²C-bus access is explained in Figure 3. The I²C-bus master writes the TDA19971 address and the subaddress to access the specific register, then it writes the data.

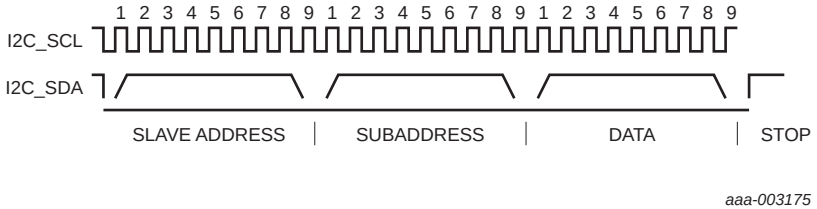

Fig 3. I²C-bus access

The I²C-bus is a separate bus to the DDC-bus, ensuring that I²C-bus programming of the TDA19971's registers does not influence DDC-bus operation.

8.5.2 Power management

The following 4 power modes are available:

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- Low-power mode:
  - Power-off mode: no supplies are available
  - EDID-only mode: only +5 V from the source available
  - pin RSTN = LOW: all supplies available, activity detection is not available
  - Idle mode: all supplies are available and there is no HDMI input. As a power-saving feature, Idle mode is automatically selected when there is no activity on the inputs. When activity is detected, Operating mode wake-up is automatically selected
- Operating mode: the device is fully functional

Remark: for low-power application or new SoC video interface, a 2.5 V supply voltage can be applied on $V_{DD(IO)(3V3)}$ pins.

8.6 CEC

TDA19971 with its embedded CEC block provides a complete solution to enable Consumer Electronic Control (CEC) in product (DSC, DVC, PMP, UM PC). This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials). CEC capability allows AV products (CEC enable) to communicate together over the home appliance network which for instance could be controlled using only one remote control.

The CEC block manages low-level transactions (compliant to CEC timing specification) over the one bidirectional line. It translates CEC protocol in I^2C-bus for the host processor and vice versa. It manages CEC message reception and transmission compliant to CEC protocol and provides the message to the system microcontroller (host processor).

For power consumption optimization purpose CEC could be enabled or disabled through I^2C-bus register.

8.6.1 Features

- Receive and transmit CEC messages to host processor
- Supports multiple CEC logical addresses
- Supports CEC messages up to 16 bytes long
- Programmable retry count
- Comprehensive arbitration and collision handling

8.6.2 CEC interrupt

Pin INT is used by TDA19971 to warn the host processor that HDMI or CEC events (for example: CEC message is available to read) have occurred.

Software interrupt status register reads determine which block between HDMI or CEC has raised the interruption before processing it.

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9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDAH(RX)(3V3)}$	receiver HDMI analog supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DDA(PLL)(3V3)}$	PLL analog supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DDAH(RX)(1V8)}$	receiver HDMI analog supply voltage (1.8 V)		–0.5	+2.5	V
$V_{DDA(DCPLL)(1V8)}$	deep color PLL analog supply voltage (1.8 V)		–0.5	+2.5	V
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)	standard 3.3 V I/O	–0.5	+4.6	V
		standard 2.5 V I/O	–0.5	+4.6	V
$V_{DDA(AUDPLL)(1V8)}$	audio PLL analog supply voltage (1.8 V)		–0.5	+2.5	V
$V_{DDA(XTAL)(1V8)}$	crystal analog supply voltage (1.8 V)		–0.5	+2.5	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		–0.5	+2.5	V
V_{ia}	analog input voltage	HDMI input	–0.5	$V_{DDAH(RX)(3V3)}$ + 0.5	V
		HDMI input clock	–0.5	$V_{DDA(PLL)(3V3)}$ + 0.5	V
V_I	input voltage	5 V tolerance I/O pins	–0.5	+6	V
		other digital I/O pins	–0.5	$V_{DD(IO)(3V3)}$ + 0.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	125	°C
HDMI input pins: RX_D0+, RX_D0–, RX_D1+, RX_D1–, RX_D2+, RX_D2–, RX_C+, RX_C–, RX_HPD, RX_DDC_DAT, RX_DDC_CLK, RX_5V and CEC					
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 class 4 (contact discharge)	–8	+8	kV
All pins:					
V_{ESD}	electrostatic discharge voltage	ANSI/ESDA/JEDEC JS-001 (HBM) [1]	–2	+2	kV
		JESD22-C101 (FCDM) [2]	–0.5	+0.5	kV

[1] It withstands at least class 2 of ANSI/ESDA/JEDEC JS-001 standard.

[2] It withstands at least class III of JEDEC standard.

10. Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air according to JEDEC 4L board (with 45 thermal vias on PCB heat sink)	22.3	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		9.3	K/W

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11. Characteristics

Table 11. Characteristics

T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDAH(RX)(3V3)}$	receiver HDMI analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDA(PLL)(3V3)}$	PLL analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDAH(RX)(1V8)}$	receiver HDMI analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDA(DCPLL)(1V8)}$	deep color PLL analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)	standard 3.3 V I/O	3.0	3.3	3.6	V
		standard 2.5 V I/O	2.25	2.5	2.75	V
$V_{DDA(AUDPLL)(1V8)}$	audio PLL analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDA(XTAL)(1V8)}$	crystal analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.65	1.8	1.95	V
$I_{DDA(3V3)}$	analog supply current (3.3 V)	Operating mode				
		720p at 60 Hz	-	95[1]	112[2]	mA
		1080p at 60 Hz	-	96[1]	113[2]	mA
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	97[1]	114[2]	mA
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	0	mA
		pin RSTN = LOW	-	0.5	0.7	mA
		Idle mode; I^2C-bus; EDID; activity detection and HDCP[3] memory power-up	-	7.1	7.8	mA
$I_{DDA(1V8)}$	analog supply current (1.8 V)	Operating mode				
		720p at 60 Hz	-	124[1]	141[2]	mA
		1080p at 60 Hz	-	158[1]	178[2]	mA
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	190[1]	212[2]	mA
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	0	mA
		pin RSTN = LOW	-	3.4	6.6	mA
		Idle mode; I^2C-bus; EDID; activity detection and HDCP[3] memory power-up	-	3.8	6.8	mA

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Table 11. Characteristics *...continued*

T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(IO)(3V3)}$	input/output supply current (3.3 V)	Operating mode				
		720p at 60 Hz	-	8[1]	70[2]	mA
		1080p at 60 Hz	-	15[1]	150[2]	mA
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	16[1]	158[2]	mA
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	0	mA
		pin RSTN = LOW	-	0	0	mA
		Idle mode; I^2C-bus; EDID; activity detection and HDCP[3] memory power-up	-	0	0	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)	Operating mode				
		720p at 60 Hz	-	38[1]	62[2]	mA
		1080p at 60 Hz	-	65[1]	116[2]	mA
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	120[1]	135[2]	mA
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	0	mA
		pin RSTN = LOW	-	6.4	8.1	mA
		Idle mode; I^2C-bus; EDID; activity detection and HDCP[3] memory power-up	-	9.1	11.5	mA
$\Delta V_{DD(3V3-3V3)}$	supply voltage difference between two 3.3 V supplies	start-up and established conditions	−100	-	+100	mV
$\Delta V_{DD(1V8-1V8)}$	supply voltage difference between two 1.8 V supplies	start-up and established conditions	−100	-	+100	mV

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Table 11. Characteristics *...continued*

T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{cons}	power consumption	Operating mode [4]				
		720p at 60 Hz	-	500	-	mW
		1080p at 60 Hz	-	636	-	mW
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	799	-	mW
		low-power mode				
		EDID only mode: EDID read, thanks to +5 V from the source	-	0	-	mW
		pin RSTN = HIGH	-	19	-	mW
		Idle mode; I^2C-bus; EDID; activity detection and HDCP[3] memory power-up	-	45	-	mW
P	power dissipation	Operating mode				
		720p at 60 Hz	-	547[5]	911[6]	mW
		1080p at 60 Hz	-	683[5]	1380[6]	mW
		1080p at 60 Hz; Deep Color 36 bits per pixel	-	848[5]	1515[6]	mW
Clock output timing pins: V_CLK and A_CLK						
$f_{clk(max)}$	maximum clock frequency	pin V_CLK	-	-	165	MHz
		pin A_CLK	-	-	24.5	MHz
δ_{clk}	clock duty cycle	pin V_CLK	40	50	60	%
		pin A_CLK	-	50	-	%
Output timing pins: VP[23:0], HS/HREF, VS/VREF and DE/FREF_3D; f_s = 165 MHz; C_L = 10 pF; $V_{DD(IO)(3V3)}$ = 3.3 V; see Figure 4 and Figure 5; formats RGB4:4:4, YCbCr 4:4:4 and YCbCr 4:2:2						
$t_{d(clk-data)}$	clock to data delay time	clk_delay = 1	-	-	4.9	ns
		clk_delay = 2	-	-	4.0	ns
		clk_delay = 3	-	-	3.2	ns
		clk_delay = 4	-	-	2.4	ns
		clk_delay = 5	-	-	1.6	ns
		clk_delay = 6	-	-	0.8	ns
$t_{h(o)}$	output hold time	clk_delay = 1	1.0	-	-	ns
		clk_delay = 2	0.5	-	-	ns
		clk_delay = 3	–0.1	-	-	ns
		clk_delay = 4	–0.7	-	-	ns
		clk_delay = 5	–1.5	-	-	ns
		clk_delay = 6	–2.8	-	-	ns

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Table 11. Characteristics *...continued*

T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output timing pins: VP[23:0], HS/HREF, VS/VREF and DE/FREF_3D; f_s = 165 MHz; C_L = 10 pF; $V_{DD(IO)(3V3)}$ = 3.3 V; see Figure 4 and Figure 5; formats CCIR656						
$t_{d(clk-data)}$	clock to data delay time	clk_delay = 0	-	-	1.4	ns
		clk_delay = 1	-	-	0.6	ns
		clk_delay = 2	-	-	0.1	ns
		clk_delay = 3	-	-	−0.4	ns
		clk_delay = 4	-	-	−0.9	ns
$t_{h(o)}$	output hold time	clk_delay = 0	−0.3	-	-	ns
		clk_delay = 1	−1.0	-	-	ns
		clk_delay = 2	−2.2	-	-	ns
		clk_delay = 3	−3.5	-	-	ns
		clk_delay = 4	−4.6	-	-	ns
Dual edge output timing pins: VP[23:0], HS/HREF, VS/VREF and DE/FREF_3D; f_s = 165 MHz; C_L = 10 pF; $V_{DD(IO)(3V3)}$ = 3.3 V; see Figure 6; formats CCIR656						
$t_{d(clk-data)}$	clock to data delay time	clk_delay = 0	-	-	5.0	ns
		clk_delay = 1	-	-	4.2	ns
		clk_delay = 2	-	-	3.4	ns
		clk_delay = 3	-	-	2.6	ns
		clk_delay = 4	-	-	1.8	ns
		clk_delay = 5	-	-	1.0	ns
		clk_delay = 6	-	-	0.3	ns
$t_{h(o)}$	output hold time	clk_delay = 0	1.1	-	-	ns
		clk_delay = 1	0.6	-	-	ns
		clk_delay = 2	0.1	-	-	ns
		clk_delay = 3	−0.4	-	-	ns
		clk_delay = 4	−1.2	-	-	ns
		clk_delay = 5	−2.2	–	-	ns
		clk_delay = 6	−3.4	-	-	ns
Output timing pins: AP[3:0], A_WS with respect to A_CLK; f_{clk} = 12.288 MHz; C_L = 10 pF; $V_{DD(IO)(3V3)}$ = 3.3 V; see Figure 7						
$t_{d(clk-data)}$	clock to data delay time		-	-	1	ns
$t_{h(o)}$	output hold time		−1.5	-	-	ns
LV-TTL digital output pins: VP[23:0], V_CLK, AP[3:0], A_WS, A_CLK, HS/HREF, VS/VREF and DE/FREF_3D; C_L = 10 pF; $V_{DDO(3V3)}$ = 3.3 V						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	2.4	-	-	V
I_{LOZ}	OFF-state output leakage current	high-impedance state	−100	0	+100	µA
LV-TTL digital output pins: VP[23:0], V_CLK, AP[3:0], A_WS, A_CLK, HS/HREF, VS/VREF and DE/FREF_3D; C_L = 10 pF; $V_{DDO(3V3)}$ = 2.5 V						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	2.2	-	-	V

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Table 11. Characteristics *...continued*

T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LOZ}	OFF-state output leakage current	high-impedance state	−100	0	+100	µA
HDMI input pins: RX_C+ and RX_C−						
$V_{I(dif)}$	differential input voltage	R_{R12K} = 12 kΩ ± 1 %	150	-	1200	mV
f_{clk}	clock frequency		20	-	235	MHz
HDMI input pins: RX_D0+, RX_D0−, RX_D1+, RX_D1−, RX_D2+ and RX_D2−						
$V_{I(dif)}$	differential input voltage	R_{R12K} = 12 kΩ ± 1 %	150	-	1200	mV
I²C-bus pins: I2C_SCL and I2C_SDA						
V_{IL}	LOW-level input voltage	standard 3.3 V I/O	-	-	0.9	V
		standard 2.5 V I/O	-	-	0.675	V
V_{IH}	HIGH-level input voltage	standard 3.3 V I/O	2.52	-	-	V
		standard 2.5 V I/O	1.925	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
C_i	capacitance for each I/O pin		-	-	2.5	pF
CEC-bus pin: CEC						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	3.63	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.6	V
I_{LOZ}	OFF-state output leakage current	high-impedance state	-	-	1.8	µA
C_i	capacitance for each I/O pin		-	-	10	pF
DDC I²C-bus pins: RX_DDC_CLK and RX_DDC_DAT[7]						
V_{IL}	LOW-level input voltage		-	-	1.5	V
V_{IH}	HIGH-level input voltage		2.5	-	5.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency	Standard-mode	-	-	100	kHz
		Fast-mode	-	-	400	kHz
C_i	capacitance for each I/O pin		-	-	10	pF
Crystal oscillator						
f_{xtal}	crystal frequency		-	27	-	MHz
Δf_{xtal}	crystal frequency accuracy		−100	-	+100	ppm
$C_{L(xtal)}$	crystal load capacitance		-	16	-	pF
C_{shunt}	shunt capacitance		-	-	7	pF
C_{ext}	external capacitance	[8]	-	18	-	pF
C_I	input capacitance	pin XTAL_IN	-	-	3.5	pF
ESR	equivalent series resistance		-	-	60	Ω

[1] At 30% activity + typical TMDS swing.

[2] Pixel ON/OFF activity + maximum TMDS swing + process/voltage/temperature deviations.

[3] HDCP decoding is only supported by TDA19971A.

[4] At 30 % activity on video port output, add 132 mW for a HDMI input with typical TMDS swing.

[5] Removed typical power consumption 112 mW on HDMI source; added power consumption 27 mW on RX_5V pin from source.

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[6] Removed maximum power consumption 151 mW on HDMI source; added power consumption 27 mW on RX_5V pin from source.

[7] 5 V tolerant.

[8] Values should be chosen smaller so to the increase of PCB layout parasitics capacitance.

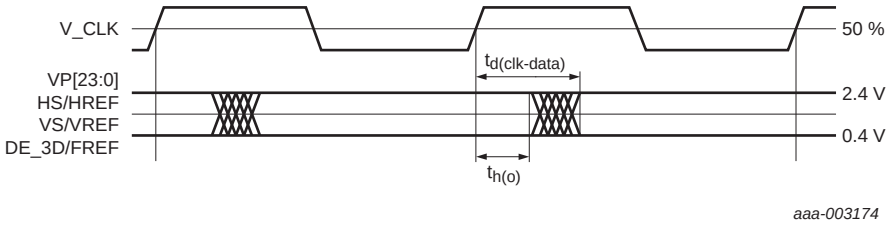

Fig 4. Output timing diagram on video bus regarding V_CLK

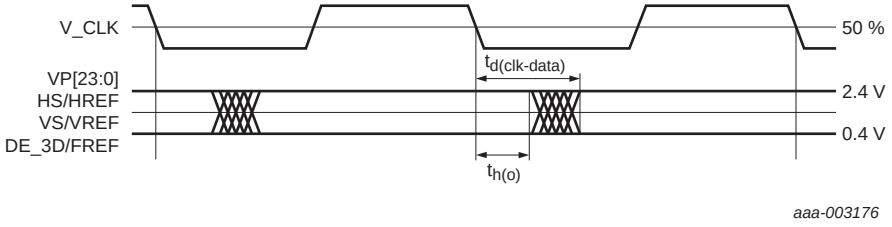

Fig 5. Output timing diagram on video bus regarding inverted V_CLK

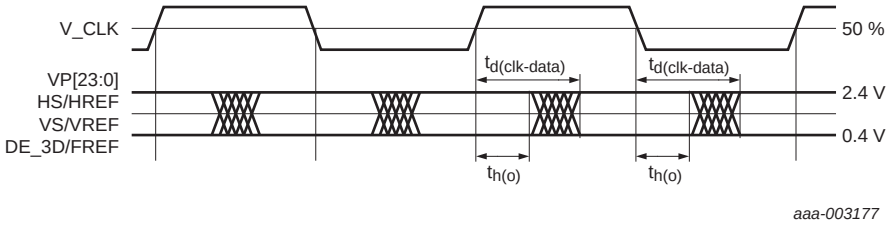

Fig 6. Dual edge output timing diagram on video bus regarding V_CLK

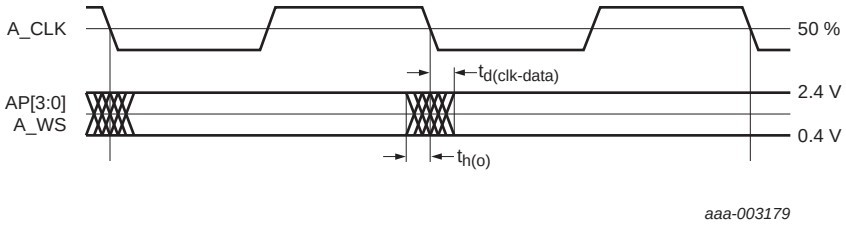

Fig 7. Output timing diagram on audio bus regarding A_CLK

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12. Example of supported video formats

Table 12. Example of supported video formats

Standard	Format	Total pixels × total lines	Horizontal rate (kHz)	Pixel clock rate (MHz)[1]
576i[2]	1440 × 576i 50 Hz	1728 × 625	15.750	27.000[3]
480i[4]	1440 × 480i 59.94 Hz	1716 × 525	15.734	27.000[3]
	1440 × 480i 60 Hz	1716 × 525	15.750	27.027[3]
576p	720 × 576p 50 Hz	864 × 625	31.250	27.000
480p	720 × 480p 59.94 Hz	858 × 525	31.469	27.000
	720 × 480p 60 Hz	858 × 525	31.500	27.027
720p	1280 × 720p 50 Hz	1980 × 750	37.500	74.250
	1280 × 720p 59.94 Hz	1650 × 750	44.955	74.176
	1280 × 720p 60 Hz	1650 × 750	45.000	74.250
1080i	1920 × 1080i 50 Hz	2640 × 1125	28.125	74.250
	1920 × 1080i 59.94 Hz	2200 × 1125	33.716	74.176
	1920 × 1080i 60 Hz	2200 × 1125	33.750	74.250
1080p	1920 × 1080p 50 Hz	2640 × 1125	56.250	148.500
	1920 × 1080p 59.94 Hz	2200 × 1125	67.433	148.352
	1920 × 1080p 60 Hz	2200 × 1125	67.500	148.500
0.31M3 VGA	640 × 480p 60 Hz	800 × 525	31.469	25.175
	640 × 480p 72 Hz	832 × 520	37.861	31.500
	640 × 480p 75 Hz	840 × 500	37.500	31.500
	640 × 480p 85 Hz	832 × 509	43.269	36.000
0.48M3 SVGA	800 × 600p 60 Hz	1056 × 628	37.879	40.000
	800 × 600p 72 Hz	1040 × 666	48.077	50.000
	800 × 600p 75 Hz	1056 × 625	46.875	49.500
	800 × 600p 85 Hz	1048 × 631	53.674	56.250
0.79M3 XGA	1024 × 768p 60 Hz	1344 × 806	48.363	65.000
	1024 × 768p 70 Hz	1328 × 806	56.476	75.000
	1024 × 768p 75 Hz	1312 × 800	60.023	78.750
	1024 × 768p 85 Hz	1376 × 808	68.677	94.500
0.98M9	1280 × 768p 60 Hz	1664 × 798	47.776	79.500
	1280 × 768p 75 Hz	1696 × 805	60.289	102.250
	1280 × 768p 85 Hz	1712 × 809	68.633	117.500
1.23M3	1280 × 960p 60 Hz	1800 × 1000	60.000	108.000
1.31M4 SXGA	1280 × 1024p 60 Hz	1688 × 1066	63.981	108.000
	1280 × 1024p 75 Hz	1688 × 1066	79.976	135.000
	1280 × 1024p 85 Hz[5]	1728 × 1072	91.146	157.500
1.04M9	1360 × 768p 60 Hz	1792 × 795	47.712	85.500
1.47M3-R	1400 × 1050p 60 Hz	1560 × 1080	64.744	101.000
1.47M3	1400 × 1050p 60 Hz	1864 × 1089	65.317	121.750
1.29MA	1440 × 900p 60 Hz	1904 × 934	55.935	106.500

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Table 12. Example of supported video formats *…continued*

Standard	Format	Total pixels × total lines	Horizontal rate (kHz)	Pixel clock rate (MHz)[1]
1.92M3 UXGA	1600 × 1200p 60 Hz[5]	2160 × 1250	75.000	162.000
1.76MA-R	1680 × 1050p 60 Hz	1840 × 1080	64.674	119.000
2.30MA-R[6]	1920 × 1200p 60 Hz	2080 × 1235	74.038	154.000

[1] Pixel clock rate corresponds to V_CLK output for 4:4:4 format and 4:2:2 semi-planar; V_CLK / 2 for 4:2:2 ITU-R BT.656 format. The pixel clock rate can be determined by:

a) Total pixels × total lines × frame rate for the progressive format.

b) Total pixels × total lines × frame rate / 2 for the interlaced format.

In ITU-R BT.656, the maximum pixel clock rate is 82.5 Mpixel/s.

[2] Also referred to as PAL (Phase Alternating Line).

[3] Pixel-doubling.

[4] Also referred to as NTSC (National Television Standards Committee).

[5] Only supports Deep Color mode 30 bits per pixel.

[6] Sometimes also referred to as WUXGA (Wide Ultra eXtended Graphics Array).

Table 13. Examples of 3D video formats timing supported

Resolution	3D transmission type
1280 × 720p at 23.98 Hz and 24 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1280 × 720p at 25 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1280 × 720p at 29.97 Hz and 30 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1280 × 720p at 50 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1280 × 720p at 59.94 Hz and 60 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080i at 50 Hz[1]	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080i at 59.94 Hz and 60 Hz[1]	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080p at 23.98 Hz and 24 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080p at 25 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080p at 29.97 Hz and 30 Hz	Frame Packing, Side-by-Side (Half), Top-and-Bottom
1920 × 1080p at 50 Hz	Side-by-Side (Half), Top-and-Bottom
1920 × 1080p at 59.94 Hz and 60 Hz	Side-by-Side (Half), Top-and-Bottom

[1] In interlaced format for Frame Packing DE/FREF_3D signal cannot be used to identify fields (Odd Left, Odd Right, Even Left, Even Right).

TDA19971 support other 3D video formats so software implementation can be considered on request.

13. Application information

For a complete application diagram, see the application note.

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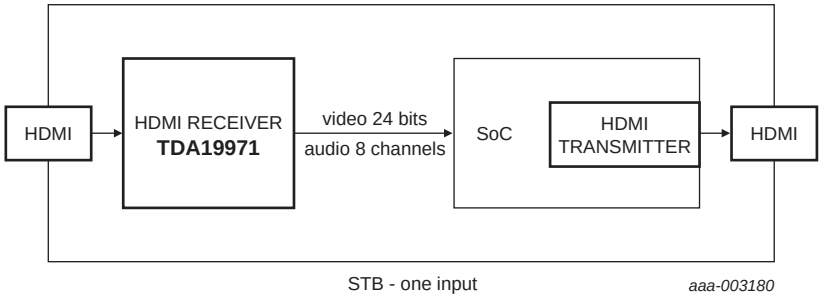

Fig 8. Single Rx input for box HVQFN72

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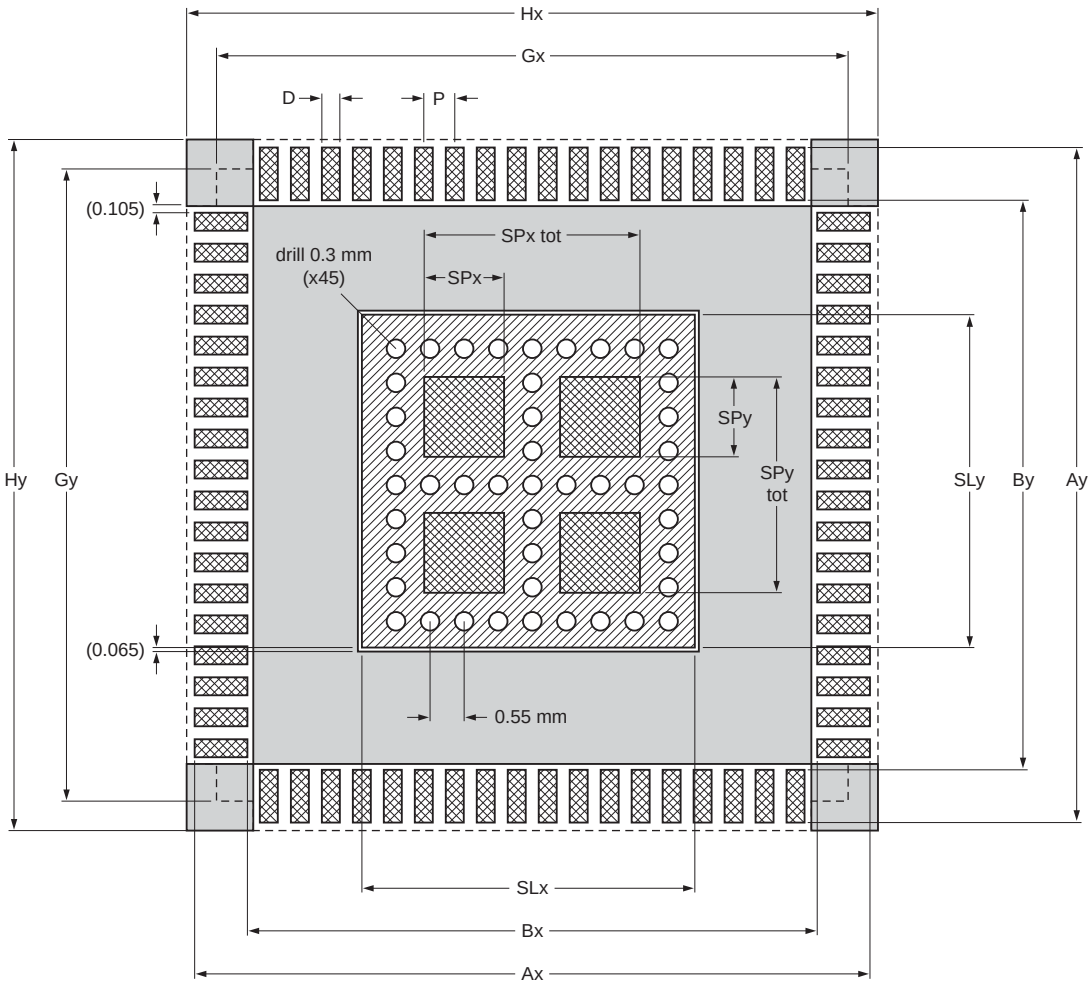
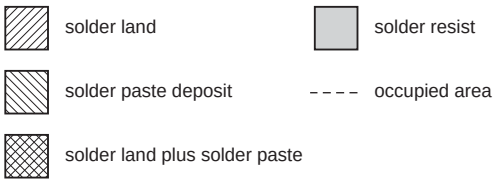
14. Footprint information for reflow soldering

Footprint information for reflow soldering of HVQFN72 package **SOT813-4**





Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	10.90	10.90	9.20	9.20	0.85	0.29	5.50	5.50	3.50	3.50	1.30	1.30	10.20	10.20	11.15	11.15

Issue date ~~12-08-31~~ 12-11-26 *sot813-4_fr*

Fig 9. Footprint SOT813-4 (HVQFN72)

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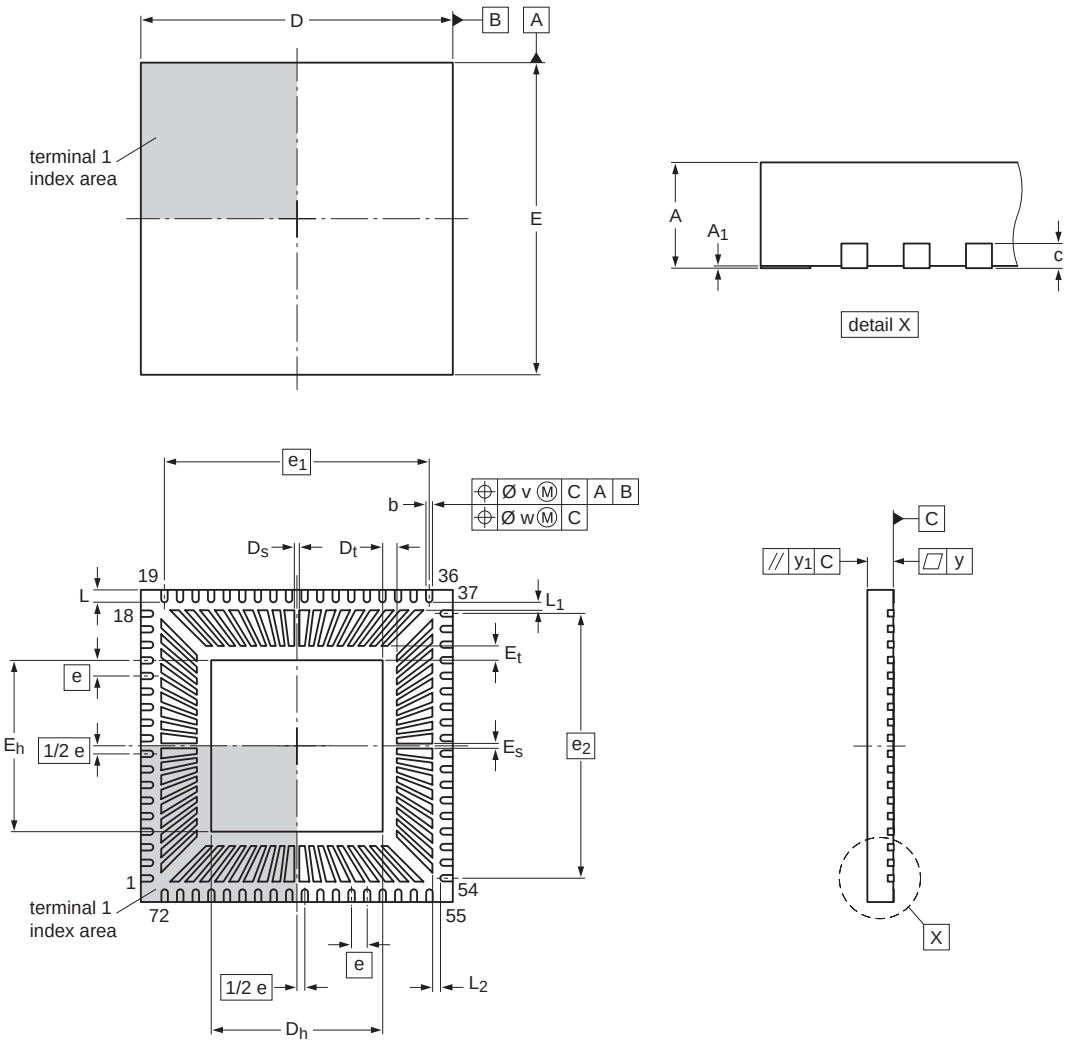
15. Package outline

HVQFN72: plastic thermal enhanced very thin quad flat package; no leads; 72 terminals; body 10 x 10 x 0.85 mm **SOT813-4**



y1
0.1

Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	$D^{(1)}$	D_h	D_s	D_t	$E^{(1)}$	E_h	E_s	E_t	e	e_1	e_2	L	L_1	L_2	v	w	y
mm	max	1.00	0.05	0.30		10.1	5.65	0.21	0.50	10.1	5.65	0.21	0.50				0.50					
	nom	0.85	0.02	0.21	0.2	10.0	5.50	0.16	0.45	10.0	5.50	0.16	0.45	0.5	8.5	8.5	0.40	0.25	0.25	0.1	0.05	0.05
	min	0.80	0.00	0.18		9.9	5.35	0.11	0.40	9.9	5.35	0.11	0.40				0.30					

Notes
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included
2. Mold flash on exposed inner terminals is allowed

sot813-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT813-4		MO-220				~~11-10-27~~ 11-11-15

Fig 10. Package outline SOT813-4 (HVQFN72)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.

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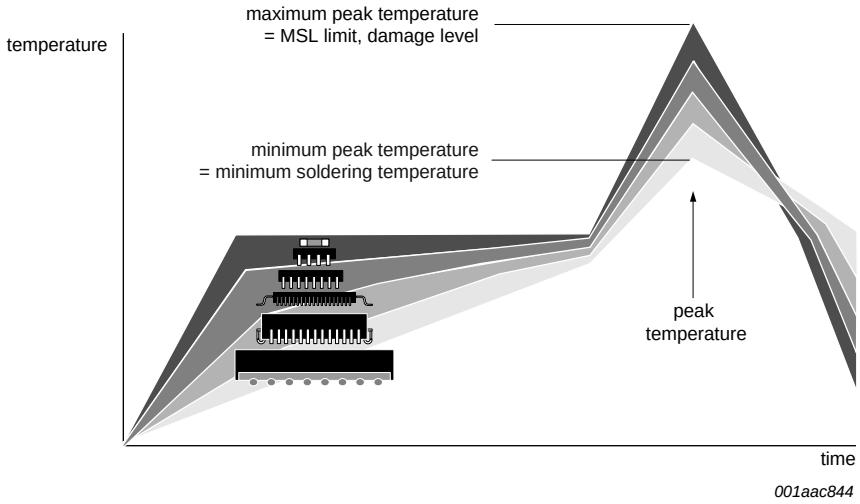

MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 16. Abbreviations

Acronym	Description
ACR	Audio Clock Regeneration
AV	Audio Video
AVN	Audio Video Navigator
AVR	Audio Video Receiver
BOM	Bill Of Material
CEC	Consumer Electronics Control
CLK	CLocK
CMOS	Complementary Metal–Oxide–Semiconductor
CPU	Central Processing Unit
DAT	DATa
DDC-bus	Display Data Channel bus
DKS	Device Key Set
DSC	Digital Still Camera
DTS-HD	Digital Theater Systems High-Definition
DVC	Digital Video Camera
DVI	Digital Video Interface
EAV	End Active Video
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge

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Table 16. Abbreviations *...continued*

Acronym	Description
FCDM	Field Charged Device Model
FIFO	First In, First Out
FREF	Field REFerence
HEAC	HDMI Ethernet Audio return Channel
HBM	Human Body Model
HBR	High Bit Rate
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition TeleVision
HPD	Hot Plug Detect
HREF	Horizontal REFerence
IC	Integrated Circuit
I/O	Input/Output
KSV	Key Selection Vector
L-PCM	Linear-Pulse Code Modulation
LV-TTL	Low Voltage Transistor-Transistor Logic
PAL	Phase-Alternation Line
PC	Personal Computer
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PMP	Portable Media Player
RGB	Red Green Blue
Rx	Receiver
SAV	Start Active Video
SCK	I^2S-bus Serial ClocK
SCL	Serial CLock
SD	I^2S-bus Serial Data
SDA	Serial DAta
SoC	System On a Chip
STB	Set-Top Box
SVGA	Super Video Graphics Array
SXGA	Super eXtended Graphics Array
S/PDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
UM PC	Ultra-Mobile Personal Computer
UXGA	Ultra eXtended Graphics Array
VCR	Video Car Recorder
VGA	Video Graphics Array
VHREF	Vertical Horizontal REFerence
VREF	Vertical REFerence
WS	Word Select

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Table 16. Abbreviations *...continued*

Acronym	Description
WUXGA	Wide Ultra eXtended Graphics Array
XGA	eXtended Graphics Array
Xtal	Crystal
YCbCr	Y = Luminance, Cb = Chroma blue, Cr = Chroma red
YUV	Y = Luminance, UV= Chroma

18. References

[1] **HDMI 1.4b —** High-Definition Multimedia Interface; Specification Version 1.4b; October 11, 2011.

[2] **CEA-861D —** A DTV profile for Uncompressed High-Speed Digital Interfaces; CEA-861rDv18; 5 August 2006.

[3] **IEC-60958 —** Digital audio interface - Part 1: General; Second edition; March 2004. Digital audio interface - Part 3: Consumer applications; Second edition; January 2003.

[4] **IEC-61937 —** Digital audio interface - Interface for non-linear PCM encode audio bit stream applying IEC-60958 - Part 1: General; First edition; May 2003.

[5] **HDCP 1.4 —** High-bandwidth Digital Content Protection; Revision 1.4; 8 July 2009.

[6] **E-DDC 1.1 —** VESA Enhanced Display Data Channel Standard; Version 1.1; 24 March 2004.

[7] **DVI 1.0 —** DVI Digital Video Interface; Revision 1.0; 2 April 1999.

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19. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA19971 v.3	20130322	Product data sheet	-	TDA19971 v.2
Modifications:	• Status updated			
TDA19971 v.2	20130212	Preliminary data sheet	-	TDA19971 v.1
TDA19971 v.1	20120910	Objective data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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